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by

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Lieutenant, United States Navy

Submitted in partial fulfillment of
the requirements for the degree of

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IN

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ABSTRACT

A general method for the analog simulation of an n^{th} order digital discrete compensator in a sampled-data servo system is presented. The method employs operational amplifiers such as are found in ordinary laboratory analog computers, and relay sampling switches driven by a low frequency function generator.

The method is discussed in relation to the trend to the use of digital devices in control systems and its theoretical development in the algebra of the z-transformation is sketched. The validity of the method was proved by comparing calculated with simulated responses, showing the accuracy of the simulated system to be no less than that of the computer itself.

The usefulness of the simulated discrete compensator is shown in a general investigation of step responses for various z-plane root locations and in an investigation of a simple adaptive system.

ACKNOWLEDGEMENT

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The motivation for this project arose during a wider investigation into a digital-analog control system conducted by U. S. Naval Post-graduate School officer students at the Dalmo-Victor Company of Belmont, California, during summer 1960. The cooperation of all Dalmo-Victor personnel, and particularly the counsel and assistance of Mr. Robert McIntosh and Mr. James Cox, are gratefully appreciated.

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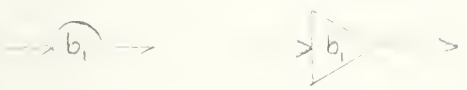
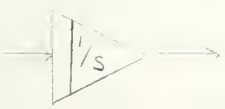
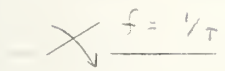
LIST OF ILLUSTRATIONS

TABLE OF SYMBOLS AND ABBREVIATIONS

Symbol	Description
a, a_1, a_{10},...,a_i,...,a_m	Coefficients of the numerator of discrete compensator
b, b_1, b_{10},...,b_i,...,b_m	Coefficients of the denominator of discrete compensator
C $\left[= C(t)\right]$, $C(s)$, $C(z)$	Output signal
$c_1(nT)$, $c_1\left[(n-1)T\right]$,...	Output time sequence
cps	Cycles per second
$D(z)$, $D_1(z)$, $D_2(z)$	Transfer function of discrete compensator
e_i	Input voltage
e_o	Output voltage
f	Frequency
$G(s)$, $G(z)$	Transfer function of plant
$G_h(s)$, $G_h(z)$	Transfer function of zero-order hold circuit
$\overline{G_hG}(z)$	Transfer function of zero-order hold circuit and plant in series
k	An integer
K	Apparent (root locus) gain
K_p	Real gain
K', K_1'	z-plane gain
m	An integer
M_p	Maximum peak overshoot
n	An integer
p_1	z-plane pole
$r(nT)$	Input time sequence
R $\left[= R(t)\right]$, $R(s)$, $R(z)$	Input signal
s	The Laplace variable

Symbol	Description
T	Interval between samples
z	z-transform variable ($= e^{sT}$)
z_1	z-plane zero
α	Second order plant inverse time constant
$\Delta\alpha$	Change in plant inverse time constant
ζ	Damping factor
τ	Sampling duration, sample pulse width, interrogation, or read out time
ω	Angular frequency (rad/second)
	Summer
	Multiplication by a constant coefficient
	Inverter
	Integrator
	Sampling switch

CHAPTER I

INTRODUCTION

The introduction of digital computers into control systems has led to the use of combinations of digital and analog devices within the same system. One interesting aspect of this use of digital devices is that of the analog simulation study. How does one go about simulating a digital computer, and all the attendant coding and decoding devices necessary for its use in the control loop, with the analog computer? This is a question that the preliminary designer faces when budgetary or equipment limitations preclude the use of digital components directly.

It is usually necessary to treat digital-analog systems within the context of sampled-data theory (1, 2, 3).* In this context, digital devices are not too difficult to simulate. A digital computation, such as multiplication or addition, or combinations of these in equations, can be programmed almost as easily in the analog computer as in the digital. Digital conversion devices such as shaft encoders, diode matrices, Shannon-Rack decoders, etc., can be simulated with unity transfer functions. These simulations are simple provided the digital computation time is short compared with the interval between samplings.

The simulation of the digital discrete compensator by analog techniques is not so simple, however. The discrete compensator gets its name from the fact that it operates on the signal only at each sampling instant. It has a z-transform which is a ratio of n^{th} order polynomials in z. Its effect is similar to that of a filter compensation in the continu-

*Numbers in parentheses, e.g., (1, 2, 3), refer to references in the Bibliography.

ous system. The difficulty in analog simulation lies in the fact that the digital realization of this discrete compensator involves storage of signals, that is, time delay, for periods of from one to n sampling periods. Such storage, while elementary in the digital computer, can be achieved only indirectly in the analog computer.

It is the purpose of this paper to present a simple technique for the direct analog simulation of a discrete compensator in a physical system and to suggest possible extensions of the technique. The paper is divided into three parts: (1) The theoretical and practical background, wherein the detailed motivation for the technique is developed; (2) A description of the general analog simulation; and, (3) A discussion of the results of two investigations designed to test the validity and usefulness of the technique.

The directness and simplicity of the technique are its major advantages. It can be used with the simplest of computers for a wide variety of laboratory or classroom problems. Changes in sampling rate, compensator coefficients, or plant constants are effected by simply changing potentiometer settings.

The development of this technique was a direct outgrowth of a project involving the development of a digital comparator for use in a simple servo loop, and subsequent digital discrete error signal compensation of a two-phase servo motor. Analog simulation of the discrete compensator became necessary when budget limitations permitted the digital mechanization of the comparator, but not that of the compensator.

CHAPTER II

THEORETICAL DEVELOPMENT

2.1 System Motivation.

A typical sampled-data system might have the configuration shown in Fig. 1. The devices shown in the blocks in Fig. 1 are typical components that might be encountered in practice. Because of their one to one equivalence the encoders can be represented by sample switches, the decoder can be represented by a zero-order hold circuit, and the comparator by an error summer. The block diagram then reduces to that of Fig. 2(a).

The location of the sampler switches can be moved across the summer and around the digital compensator, since the digital compensator only receives and operates on error signals at the sampling instants. The system diagram then becomes that of Fig. 2(b).

This is the classic discrete compensator circuit described in the literature. In arriving at it, the following assumptions are made:

(1) All encoders are interrogated at the same time, and their difference, the output of the error summer, is the error that exists at $t = nT$ (where T = the sampling or interrogation period.)

(2) That the interrogation, or read out, time (corresponding to sample pulse width τ) is short compared to T. This permits analysis on an impulse basis. It might be pointed out that this is generally valid, since interrogation time will usually be of the order of a few microseconds, whereas T will most likely be longer than a millisecond. Interrogation time might be longer if the encoder's output is serial binary, but this is treated in the next assumption.

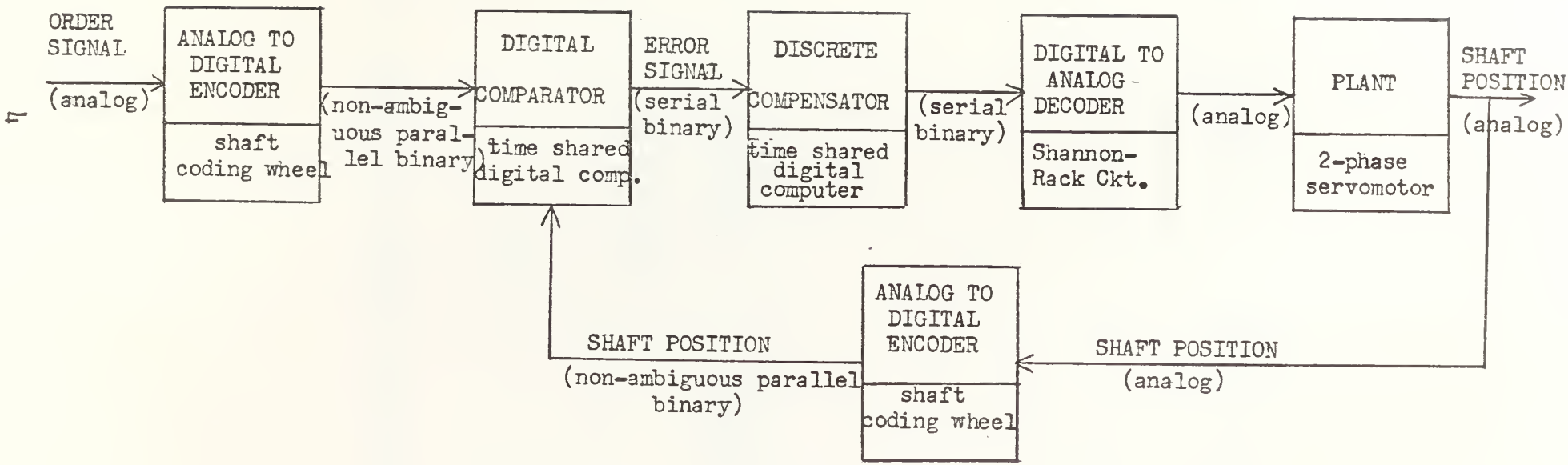
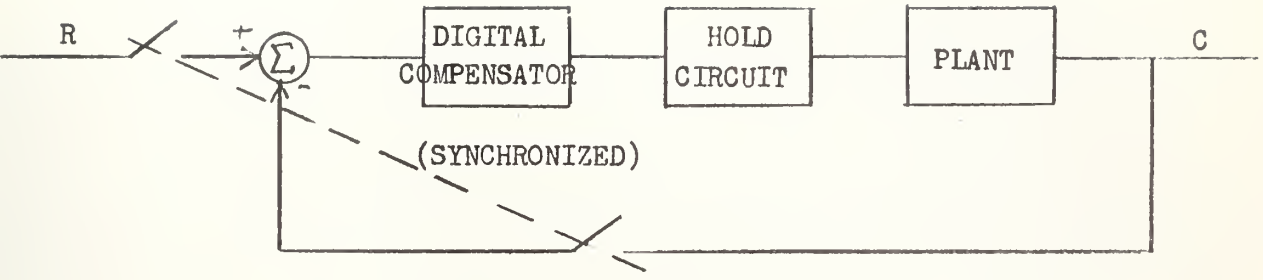
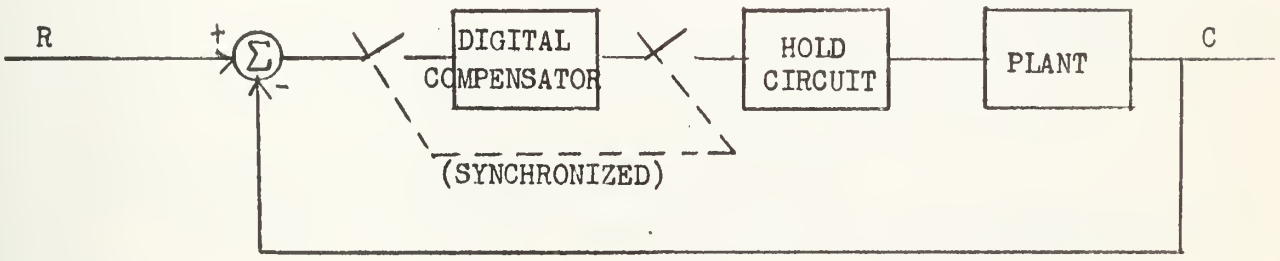


FIGURE 1. TYPICAL SAMPLED-DATA SYSTEM



(a)



(b)

FIGURE 2. SIMPLIFIED COMPENSATED SAMPLED-DATA SYSTEM

(3) Computation time in the comparator and discrete compensator is short compared with T. This could be a problem if less recent digital logic modules are used, but for most modern equipment it is not.

It would be possible, of course, to introduce the compensation between the hold circuit and the plant. This would be very close to continuous compensation. However, the output of the hold circuit is quantized, and if the assumption is made that the digital computer must be time shared (often one of the justifications for a sampled-data system), the analysis of the continuous compensation gets quite difficult and its generality is reduced. In addition, it is often true that the plant is airborne and the computer on the ground with a digital communication link between them (another justification for the sampled-data system). In this case it might be necessary to eliminate all excessive airborne components, thus the desirability of having the compensation on the ground, in the computer.

2.2 Theory of Discrete Compensator Realization.

In general, the digital discrete compensator can be represented by:

$$D(z) = \frac{a_0 + a_1 z^{-1} + a_2 z^{-2} + \ldots + a_n z^{-n}}{b_0 + b_1 z^{-1} + b_2 z^{-2} + \ldots + b_n z^{-n}}$$

$$= \frac{\sum_{k=0}^{n} a_k z^{-k}}{b_0 + \sum_{k=1}^{n} b_k z^{-k}}$$

The only restriction on the generality of this statement is that $b_0 \neq 0$.*

*Tou, J. T.; Digital and Sampled-Data Control Systems, McGraw-Hill Book Co., New York, 1949, pp 432-3.

Ragazzini and Franklin* demonstrate the realizability of D(z) in the following manner:

$$\text{Let} \qquad D(z) = \frac{a_0 + a_1 z^{-1} + a_2 z^{-2} + \ldots + a_m z^{-m}}{1 + b_1 z^{-1} + b_2 z^{-2} + \ldots + b_k z^{-k}} = \frac{C(z)}{R(z)}$$

and let D(z) contain the two factors

$$D_1(z) = \frac{1}{1 + b_1 z^{-1} + b_2 z^{-2} + \ldots + b_k z^{-k}}$$

$$D_2(z) = a_0 + a_1 z^{-1} + a_2 z^{-2} + \ldots + a_m z^{-m}$$

The block diagram for $D_1(z)$ is shown in Fig. 3. (4)

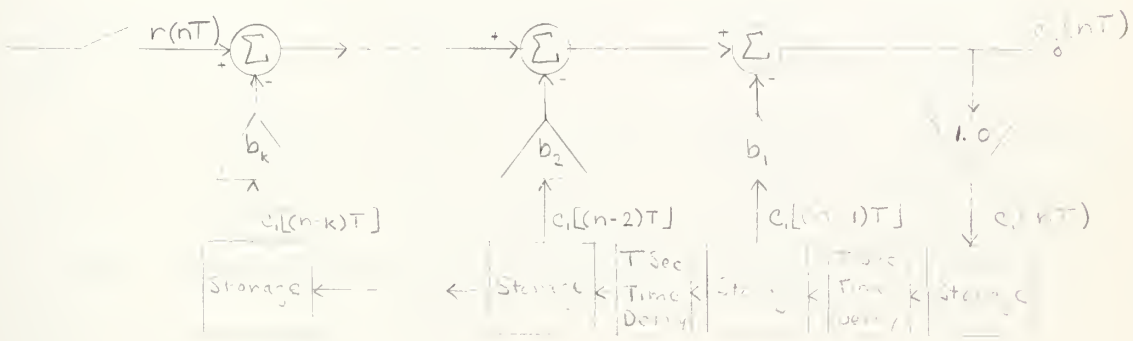


Figure 3.

The z-transform of the output sequence is $C_1(z)$ and the n^{th} pulse in the time domain is $c_1(nT)$. Each time delay is T seconds. Tracing the signal through the block diagram we see that

$$c_1(nT) = r(nT) - b_1 c_1\left[(n-1)T\right] - b_2 c_1\left[(n-2)T\right] - \ldots$$

$$r(nT) = c_1(nT) + b_1 c_1\left[(n-1)T\right] + b_2 c_1\left[(n-2)T\right] + \ldots$$

*Ragazzini, J. R., and Franklin, G. F.; Sampled-Data Control Systems, McGraw-Hill Book Co., New York, 1948, pp 76-7.

Taking the z-transform of both sides, there results

$$R(z) = C_1(z)(1 + b_1 z^{-1} + b_2 z^{-2} + \ldots + b_k z^{-k})$$

which yields $D_1(z)$.

The total output $C(z)$ is now obtained by operating on $C_1(z)$ by $D_2(z)$. $c_1(nT)$ is the present output sample and it should be operated on by a_0. Similarly, $c_1\ (n-1)T$ should be operated on by a_1. This operation on successively earlier signals is the significance of z^{-m} in the $D_2(z)$ terms. If these operations are then summed we have the desired $D(z)$. This is accomplished by the arrangement in Fig. 4.

This is one of many configurations possible to realize discrete compensation.* It has the advantage of requiring a minimum number of delay elements, and for this reason was used in this investigation.

Such a compensator could be programmed reasonably into a digital computer, and because of the possibility of storage between sampling periods, a general purpose computer could readily be time shared to handle this and other problems.

The design engineer would now desire to know how a given compensation of this sort would affect his system. Analytically, this could be obtained by taking the modified z-transform

$$C(z,m) = \frac{R(z)\ D(z)\ \overline{G_h G}\ (z,m)}{1 + D(z)\ \overline{G_h G}\ (z,m)}$$

of the system

Figure 5.

*Tou; pp 449-454.

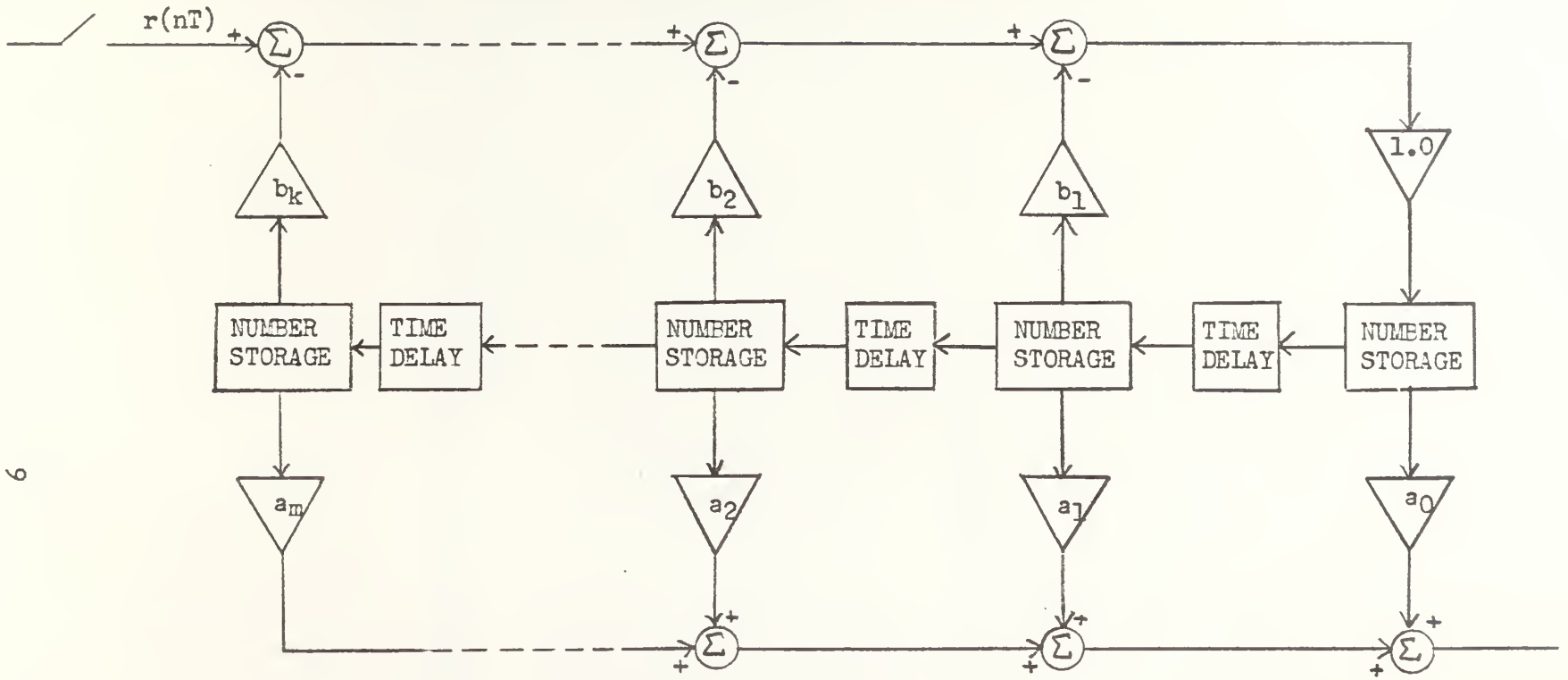


FIGURE 4. REALIZATION OF DISCRETE COMPENSATOR

where $\overline{G_h G}(z)$ and $\overline{G_h G}(z,m)$ are the z and modified-z transforms, respectively, of the zero order hold circuit and plant in series.

If D(z) is of high order, this analysis becomes quite laborious. If a digital computer is available for analysis, it might still be inconvenient to vary the program for experimental changes in the a_i and b_i of D(z). An analog computer simulation immediately suggests itself.

The chief problem involved in setting up an analog simulation is, of course, realizing D(z). Several methods have been described in the literature. Sklansky converts D(z) into an equivalent R-C network in the s-domain (5). This method has the disadvantage of an extremely laborious conversion of z-plane coefficients (the a_i and b_i) into working coefficients in the s-plane.

The difficulty in reproducing a direct analog of D(z) lies in developing a storage and delay circuit. Bigelow achieved this by using operational amplifiers with sequencing switches, and later, dekatron tubes (6, 7). Dye accomplished this delay by magnetic amplifiers (8). These methods all have the disadvantage of requiring extensive and sophisticated equipment.

2.3 Analysis of Delay Circuit.

The delay circuit used in this development was obtained from the following circuit:

Figure 6.

where $G_{hold}(s) = G_h(s) = \dfrac{1 - e^{-Ts}}{s}$, and $G(s) = \dfrac{1}{Ts}$

The z-transform of the closed loop is:

$$\frac{e_0}{e_i}(z) = \frac{\overline{G_h G}(z)}{1 + \overline{G_h G}(z)}$$

now, $$\overline{G_h G}(z) = \frac{1 - z^{-1}}{T} \mathcal{Z}\left\{\frac{1}{s^2}\right\}$$

$$= \frac{(z - 1)}{Tz} \quad \frac{Tz}{(z - 1)^2} = \frac{1}{z - 1}$$

then, $$\frac{e_0}{e_i}(z) = \frac{1 / (z - 1)}{1 + 1 / (z - 1)} = \frac{1}{(z - 1) + 1} = \frac{1}{z}$$

or, $$e_0 = e_i z^{-1}$$

which means that the output voltage is the same as the input, but delayed by T seconds. This is true provided the output is sampled, for the above is true only at the sampling instants. A graphical explanation of the above phenomenum is contained in Appendix I.

This delay circuit is simple to set up on any analog computer; requires no expensive or even unusual equipment; and is adaptable, since a change in sampling rate requires only one compensatory potentiometer setting change.

CHAPTER III

GENERAL SIMULATION OF A SECOND ORDER SYSTEM

Fig. 7 shows an analog simulation of the system of Fig. 2(b) that is valid for any order D(z) where

$$D(z) = \frac{1 + a_1 z^{-1} + a_2 z^{-2} + \ldots + a_m z^{-m}}{1 + b_1 z^{-1} + b_2 z^{-2} + \ldots + b_k z^{-k}}$$

and $$G(s) = \frac{K}{s\,(s + \alpha)}$$

with sampling frequency = 1/T.

This is an exact analog of the digital discrete compensation of Fig. 4. There is no explicit storage device in the analog simulation. Since analog information is available instantaneously, this is unnecessary. However, because this analog information is available at all times, but is correct only at t = nT (the sampling instants), there exists the requirement that the output of the compensator be sampled, and that all samplers be in synchronism. This latter requirement is easily met by using the same triggering source for the samplers.

In practice this configuration would be modified considerably, since, in general, the plant would be more complex than second order and the D(z) coefficients would have positive or negative signs. Sign changing is accomplished routinely by inserting sign changing amplifiers where necessary.

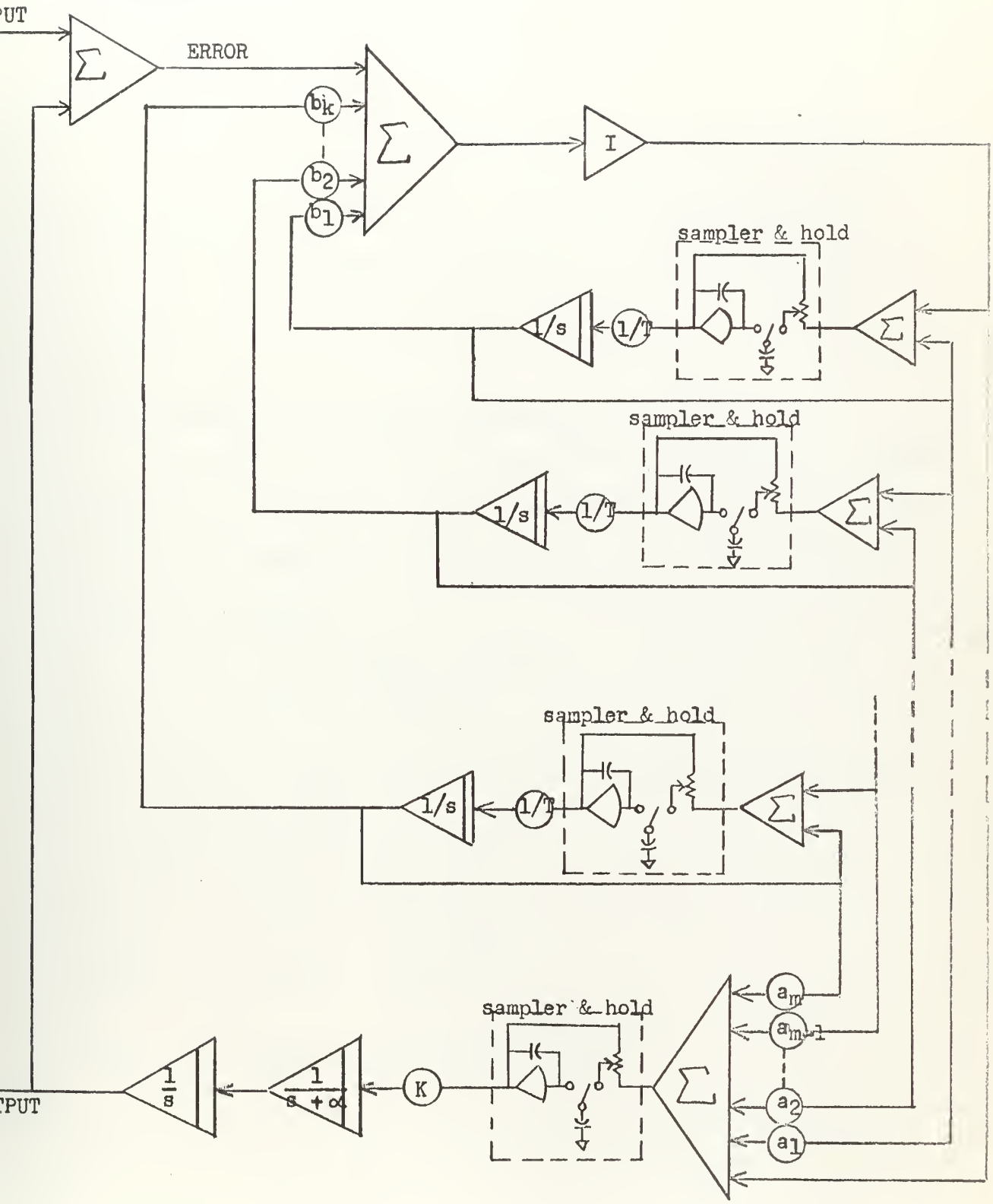


FIGURE 7. GENERAL SIMULATION OF SECOND ORDER SYSTEM

CHAPTER IV

RESULTS OF INVESTIGATIONS

4.1 Equipment.

The analog computer used was a Donner Model 3000. Two sampler and hold circuits, each containing a relay sampler triggered by a low frequency function generator and a Philbrick USA-3 operational amplifier were used. A more detailed description of these is contained in Appendix II.

4.2 Investigation of z-plane Root Locations.

To evaluate the validity and usefulness of the technique, a simple system was postulated and various first order compensations were applied to it. This permitted a relatively simple analytical check of the accuracy of the system.

A plant with the Laplace transform

$$G(s) = \frac{K}{s\,(s+1)}$$

was set up. A sampling period (T) of one second was chosen, and K = 1.0 was the initial gain.

With $$G_h(s) = \frac{1 - e^{-Ts}}{s}$$

then $$G_h G(s) = \frac{(1 - e^{-Ts})}{s^2(s+1)}$$

and $$\overline{G_h G}(z) = \frac{0.368\,(z + 0.718)}{(z-1)\,(z - 0.368)}$$

The closed loop roots for this system with no compensation (sampled error) were found on the z-plane root locus diagram in Fig. 8. If the pole at z = 0.368 is cancelled by a zero of the compensator, and another pole is introduced by the compensator, by changing the compensator pole and the

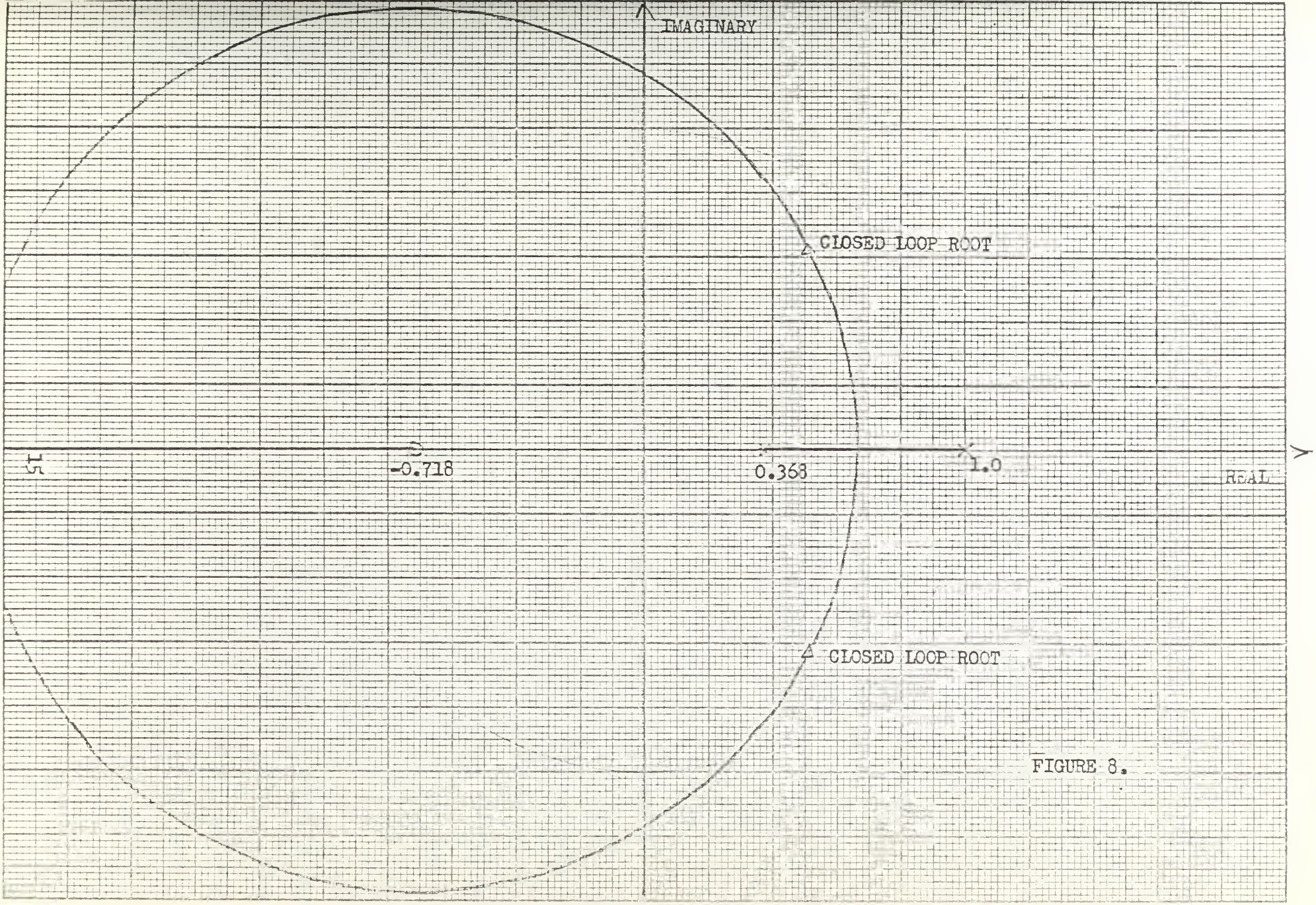

IMAGINARY
CLOSED LOOP ROOT
-0.718
0.368
1.0
REAL
CLOSED LOOP ROOT

FIGURE 8.

system gain, it is possible to produce two closed loop roots anywhere in the z-plane. This was done for most of the stable region of the z-plane with results discussed below.

Table I and Fig. 9 show the compensated root locations for the various compensations investigated. The system has, for a first order compensator using pole cancellation, the open loop transfer function:

$$D(z)\overline{G_h G}(z) = \frac{(z - 0.368)}{(z - b)} \quad \frac{K' (z + 0.718)}{(z - 0.368)(z - 1)}$$

The roots are enumerated and identified by b and K' in Table I and located in the z-plane in Fig. 9. Note that each complex root in Fig. 9 has a complementary root in the negative imaginary region. Step responses for all root locations are contained in Figs. 10 - 18. The responses for root locations 1, 2, 18, and 20 were compared against analytically computed curves with results that corresponded with an error of 5% or less. It is felt that this is, in general, sufficient accuracy for the design engineer doing preliminary work, and it is all that can be expected from the computer without chopper stabilized amplifiers and temperature stabilized components. In any event, these comparisons with the relatively laboriously calculated curves are sufficient justification for the approach, since they show that a good, quick solution of the digitally compensated plant response can be obtained for all time, not just the sampling instants, by analog simulation.

Compensating in the z-plane doesn't offer as many guide lines as does compensating in the s-plane. Among other things, constant ζ lines, which map into the z-plane as logarithmic spirals, lose their meaning there due to intersampling effects. Jury, in discussing design parameters, takes as one such parameter the maximum peak overshoot, M_p, and draws curves

for this in the z-plane.* The investigation confirmed Jury's curves and indicated that M_p might be the best simple parameter for compensation. These curves are extended in Fig. 19 for most of the z-plane.

It can be seen in Table I that there is a reasonable correlation between expected transient frequency and that observed, although this fact is of questionable usefulness as a design parameter. Nothing could be deduced from the response data that served to link root location and settling time. In general the step response becomes more heavily damped as the roots move toward the positive real axis ($0 \leq z \leq 1.0$).

Some interesting responses are produced by roots on the real axis. The presence of a negative real root causes ripple even where there is a definite positive real root (root location #6). This is true, as well, in those cases where the residue of the negative real root vanishes, e.g., the case of cancellation compensation (#s 7, 8, 9). This ripple can even cause overshoot and give the impression of underdamping (#9, 10).

Root #11 was placed at the stability limit, and produced the expected erratic phenomena with the system nonlinearities taking charge. Among these phenomena was the marked undershoot following the first overshoot. This was also noted for the complex roots located in the vicinity of $z = -1.0$ (#s 34-36, 39-44). Roots in the remote stable portions of the second quadrant near the unit circle display stable characteristics, but have far greater overshoots and undershoots than do comparable root locations for continuous systems.

Roots #45 consist of a stable positive real root and an unstable negative real root. The resulting limit cycle demonstrates this

* Jury, E. I.; Sampled-Data Control Systems, John Wiley & Sons, New York, 1958, pp 132-4.

4.3 Investigation of an Adaptive System.

An adaptive system is defined herein to be a system that changes itself to produce a better response as certain external conditions change than the same system would without the adaptive feature. In order to utilize a digital computer to effect changes to make a system adaptive, programming in advance would probably have to be employed.

As an example of this use of the digital computer, consider the following system: Assume that it is known that the time constant of the plant would change during operation due to environmental changes, such as are encountered by an aircraft or missile operating under varying velocities, densities, and temperatures, and that these changes occur between well defined limits. These changes can be measured externally to the control loop. Assume that the amount of change of the time constant is a definable function of the measured parameters, and its formulation can be programmed into a computer. Once formulated, the time constant change is then applied to the digital compensator to effect either compensator pole or zero shifts or both to compensate for the system pole and zero shift.

To investigate a system of this type it was assumed that the system was compensated by a first order compensator, D(z), where

$$D(z) = \frac{(z + a_{10})}{(z + b_{10})}$$

and that this compensation was satisfactory.

The plant has the transfer function

$$G(s) = \frac{K}{s\,(s + \alpha)}$$

The inverse of the plant time constant, α, is varied an amount $\pm \Delta\alpha$. This change manifests itself in the z-transform by:

(1) a new pole position

$$p_1 = e^{-(\alpha \pm \Delta\alpha)T}$$

(2) a new zero position

$$z_1 = \frac{e^{-(\alpha \pm \Delta\alpha)T}\,(T + 1) - 1}{T + e^{-(\alpha \pm \Delta\alpha)T} - 1}$$

(3) a new z-plane gain

$$K_1' = \frac{K'}{2}\,(T + e^{-(\alpha \pm \Delta\alpha)T} - 1)$$

The designer has at his disposal a_1 and b_1 to re-compensate for the changed conditions. If some formula of the form either

$$a_1 = f(a_{10}, b_{10}, \Delta\alpha)$$

or $$b_1 = g(a_{10}, b_{10}, \Delta\alpha)$$

or both, can be determined that will satisfactorily compensate the changed system, this formulation could be readily programmed into the digital computer. This can be called pole and zero migration.

In the investigation, an empirical approach to obtain such formulas was used. The system with initial compensation was set up on the computer and was varied an amount $\Delta\alpha$. By trial and error, compensator pole or zero migrations were introduced and the step response observed. The criterion for success was the minimum deviation of the step response

from the original uncharacterized compensated response in overshoot and rise time.

For the system investigated:

$$K = 1.00 \quad (K' = 0.368)$$

$$\alpha = 1.00$$

$$a_{10} = -0.368$$

$$b_{10} = -0.100$$

This was the compensated system with root location #3, described in the previous section. Rise time was satisfactory with $M_p = 18\%$.

Zero Migration Only.

Satisfactory response was demonstrated for $-0.6 \leq \Delta\alpha \leq 0.2$ when

$$a_1 = (a_{10} + 0.7\,\Delta\alpha)$$

Pole Migration Only.

Satisfactory response was demonstrated for $-0.4 \leq \Delta\alpha \leq 0.0$ when

$$b_1 = (b_{10} - \Delta\alpha)$$

These responses are displayed in Figs. 20 and 21.

Although a system could be envisioned with the transfer function

$$G(s) = \frac{K}{s(s + \alpha)} \qquad (1)$$

a more likely physical second order system (servomotor) would have the transfer function

$$G(s) = \frac{K_p}{s\,(1/\alpha\, s + 1)} = \frac{\alpha K_p}{s\,(s + \alpha)}$$

where K_p is the real gain of the system. K in (1) above is now a function of the plant time constant. For example, if α were decreased, the system would tend to become more oscillatory, but simultaneously, the

error signal until T seconds after the step is applied. Rise time is largely determined by the slope of the initial rise and this in turn is determined by the system gain, αK_p. If T were very much shorter than rise time this kind of compensation would be possible, but then the sampled-data system would approach being a continuous system.

However, if the gain of the system is multiplied by the new time constant, $1/\alpha_1$, where $\alpha_1 = \alpha \pm \Delta\alpha$, as the system changes, then the open loop plant transfer becomes

$$G(s) = (1/\alpha_1)\frac{\alpha_1 K_p}{s(s + \alpha_1)}$$

which is the original system investigated with $K = K_p$ = constant. This programming of the gain can be mechanized easily, utilizing the same information source from which $\Delta\alpha$ was obtained.

It should be noted that responses obtained for pole or zero migrations are satisfactory for a limited range of $\Delta\alpha$. More elaborate re-compensation by formula by combinations of pole and zero migration seems possible but was not investigated.

Table I.

Root Location		K'	P_p	ζ_T	ω_T
1	.368	.368	.43	.135	.139
2	.600	.368	.73	.132	.131
3	.100	.368	.18	--	--
4	-.100	.368	.04	--	--
5	-.300	.368	--	--	--
6	-.500	.368	--	--	--
7	-.718	.368	--	.500	--
8	-.718	.600	--	.500	--
9	-.718	.800	.07	.500	--
10	-.718	1.00	.30	.500	--
11	-.718	2.00	1.40	.454	--
12	.368	.600	.69	.174	.191
13	.100	.600	.41	.193	.195
14	-.100	.600	.24	.200	.206
15	-.300	.600	.07	--	--
16	.368	.800	.35	.196	.203
17	.100	.800	.59	.217	.222
18	-.100	.800	.42	.233	.242
19	-.300	.800	.24	.263	.264
20	-.500	.800	.14	--	--
21	.100	1.00	.76	.235	.242
22	-.100	1.00	.56	.256	.261
23	-.300	1.00	.44	.283	.286
24	-.500	1.00	.35	.313	.316

TABLE

[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	.100	1.00	.90	.280	[illegible]
27	-.100	1.20	.74	.260	.270
27	-.300	1.20	.65	.292	.302
28	-.500	1.20	.57	.322	.340
29	-.600	1.20	.55	.400	.392
30	-.650	1.20	.53	.417	.433
31	-.100	1.50	1.06	.280	.300
32	-.300	1.50	.99	.310	.326
33	-.500	1.50	.93	.340	.366
34	-.600	1.50	.91	.370	.397
35	-.650	1.50	.89	.395	.422
36	-.700	1.50	.89	.419	.463
37	-.300	1.80	1.25	.331	.343
38	-.500	1.80	1.20	.364	.390
39	-.600	1.80	1.17	.389	.410
40	-.650	1.80	1.17	.413	.431
41	-.700	1.80	1.16	.427	.464
42	-.500	2.00	1.42	.379	.399
43	-.600	2.00	1.36	.406	.413
44	-.650	2.00	1.40	.413	.439
45	-.900	1.00	.37	.500	--

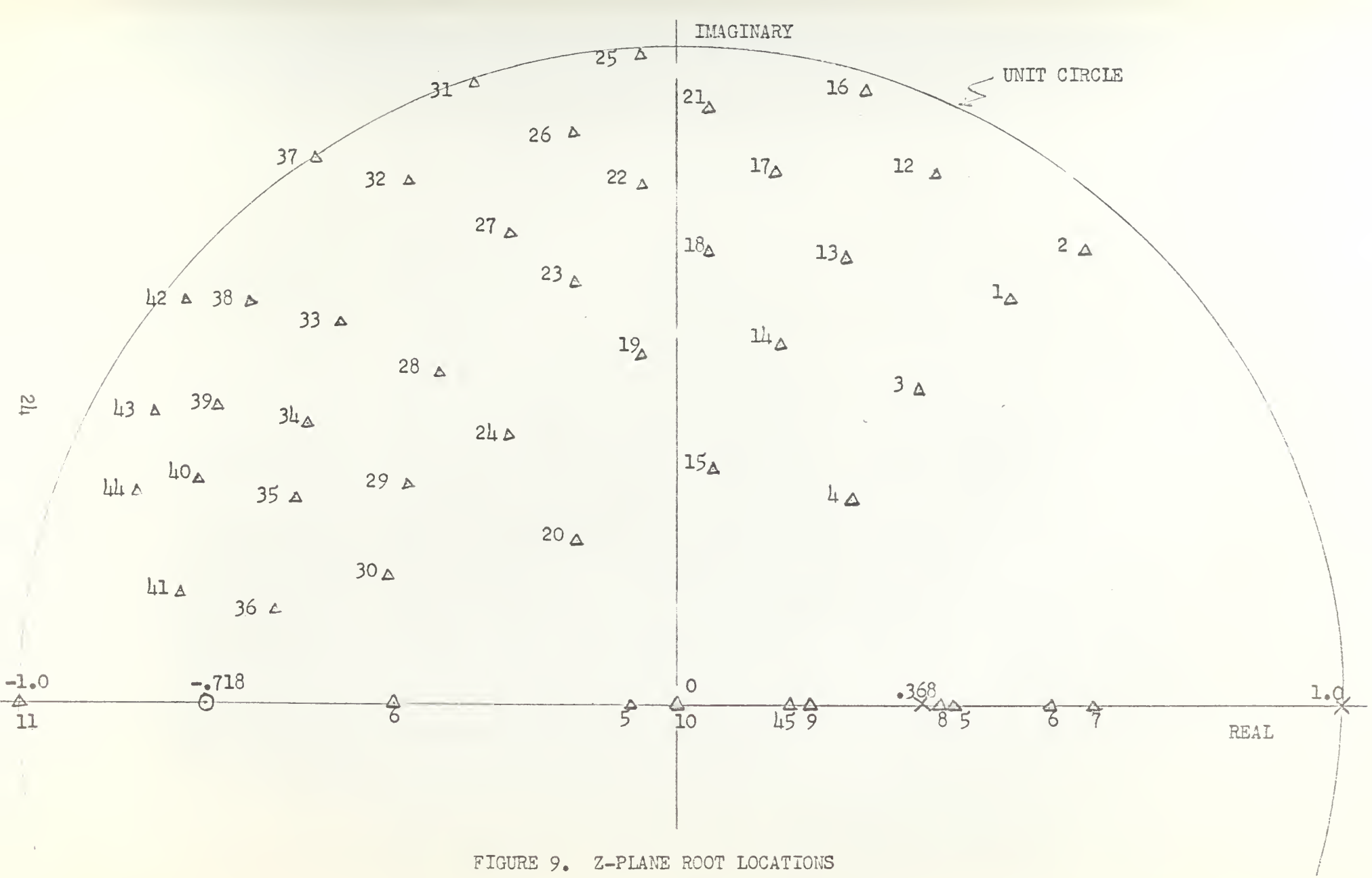


FIGURE 9. Z-PLANE ROOT LOCATIONS

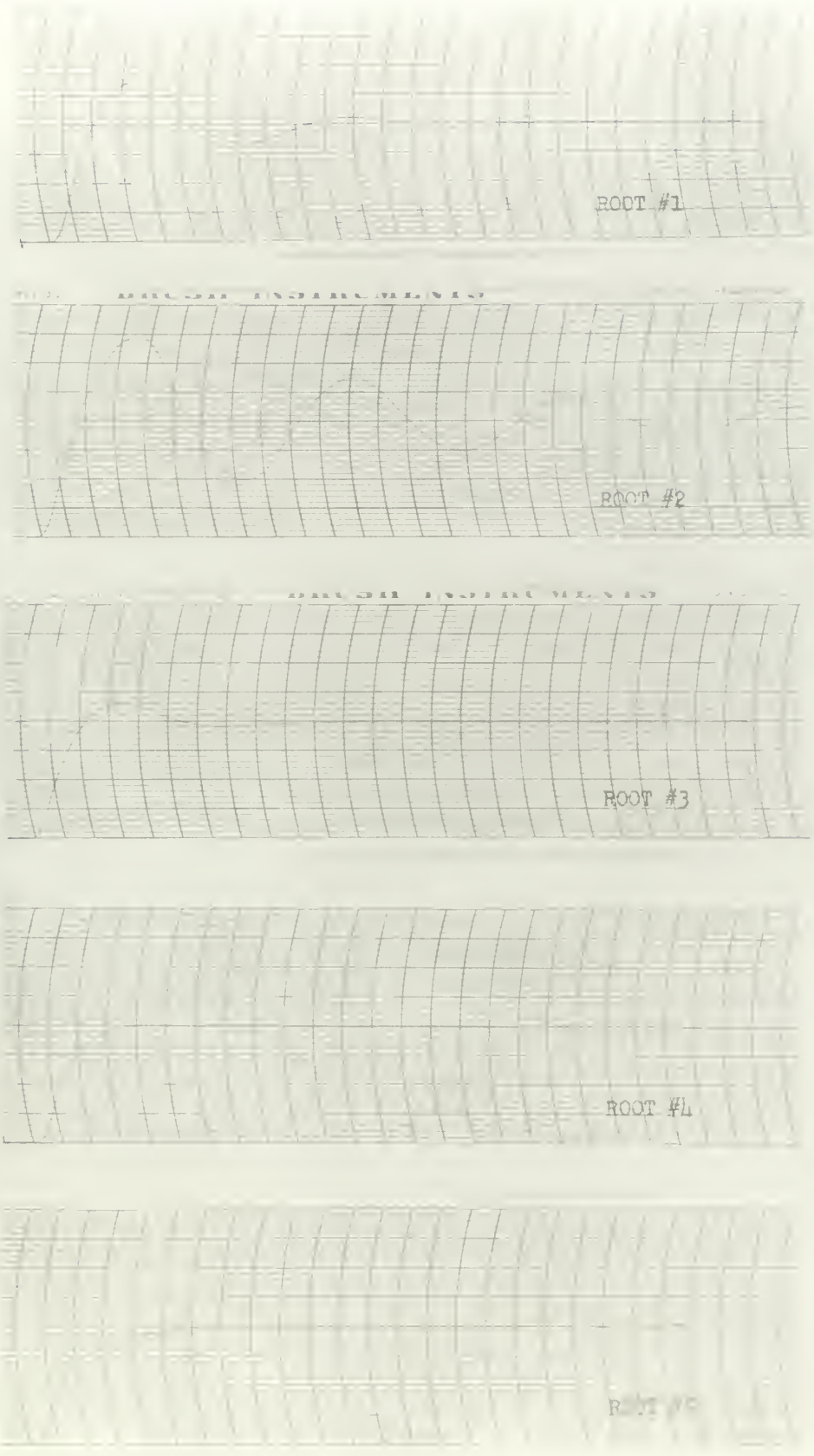


FIGURE 10. STEP RESPONSES ROOTS 1 - 5

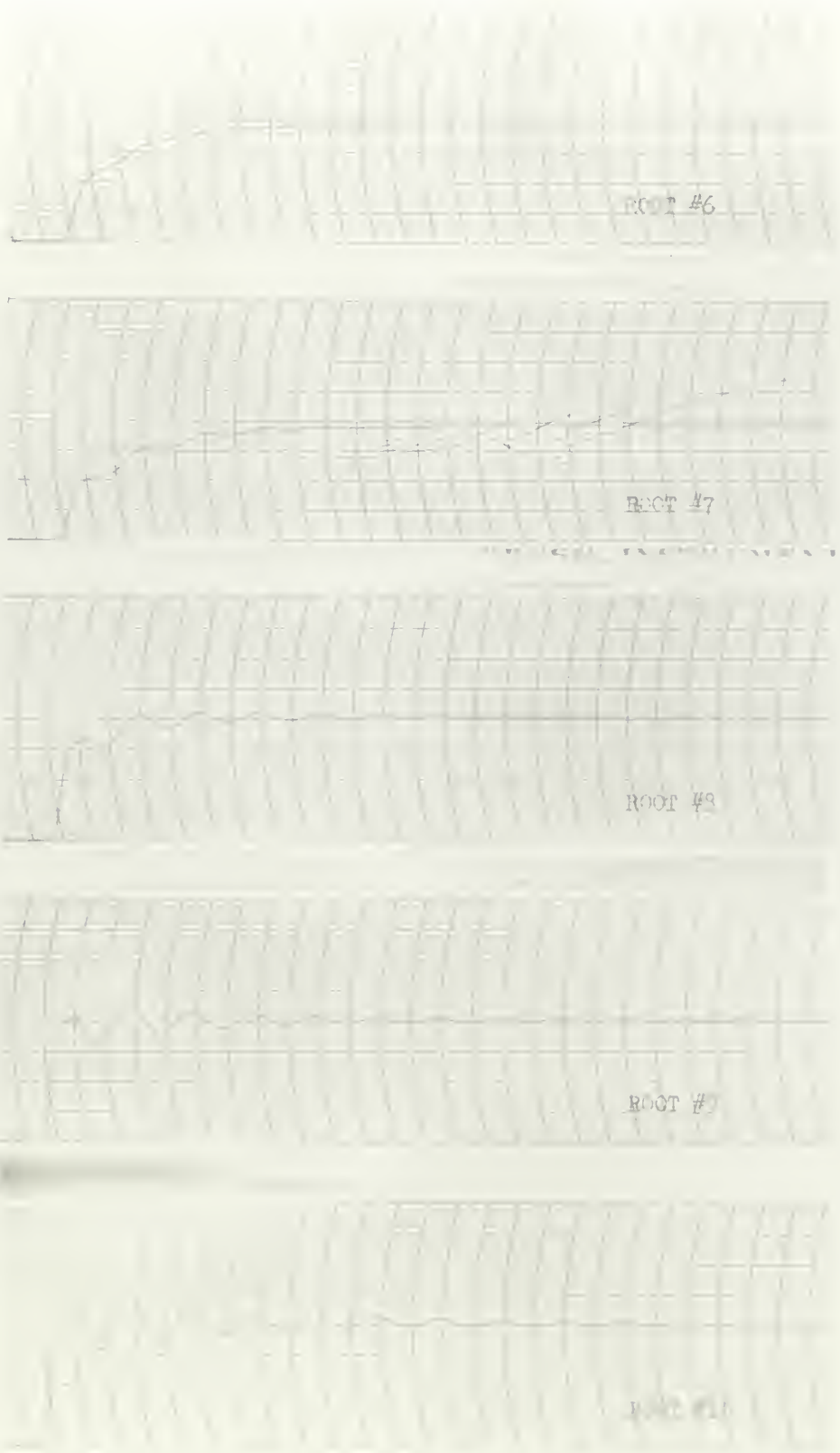


FIGURE 11. STEP RESPONSES ROOTS 6 - 10

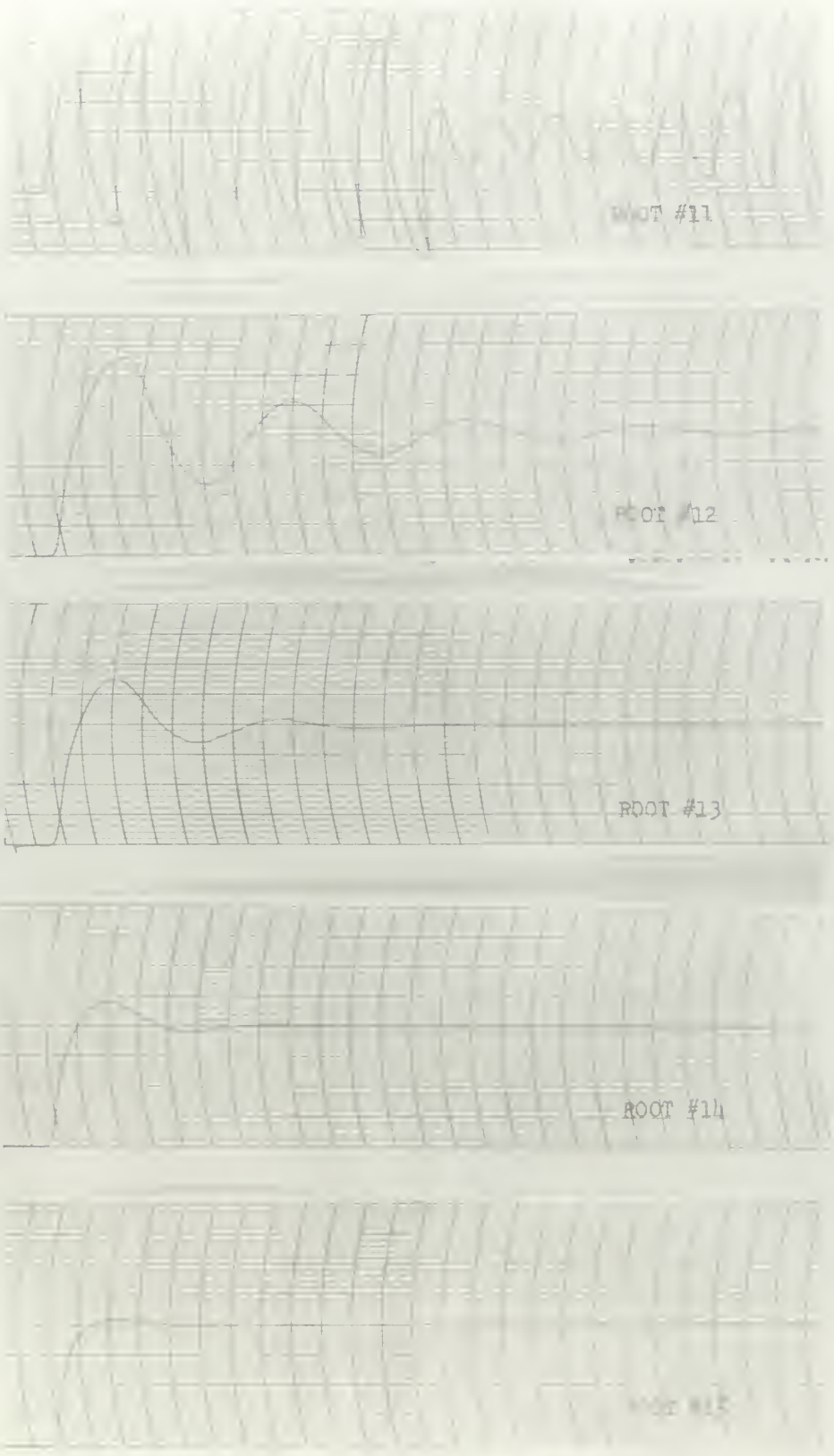


FIGURE 12. STEP RESPONSE ROOT 11 - 15

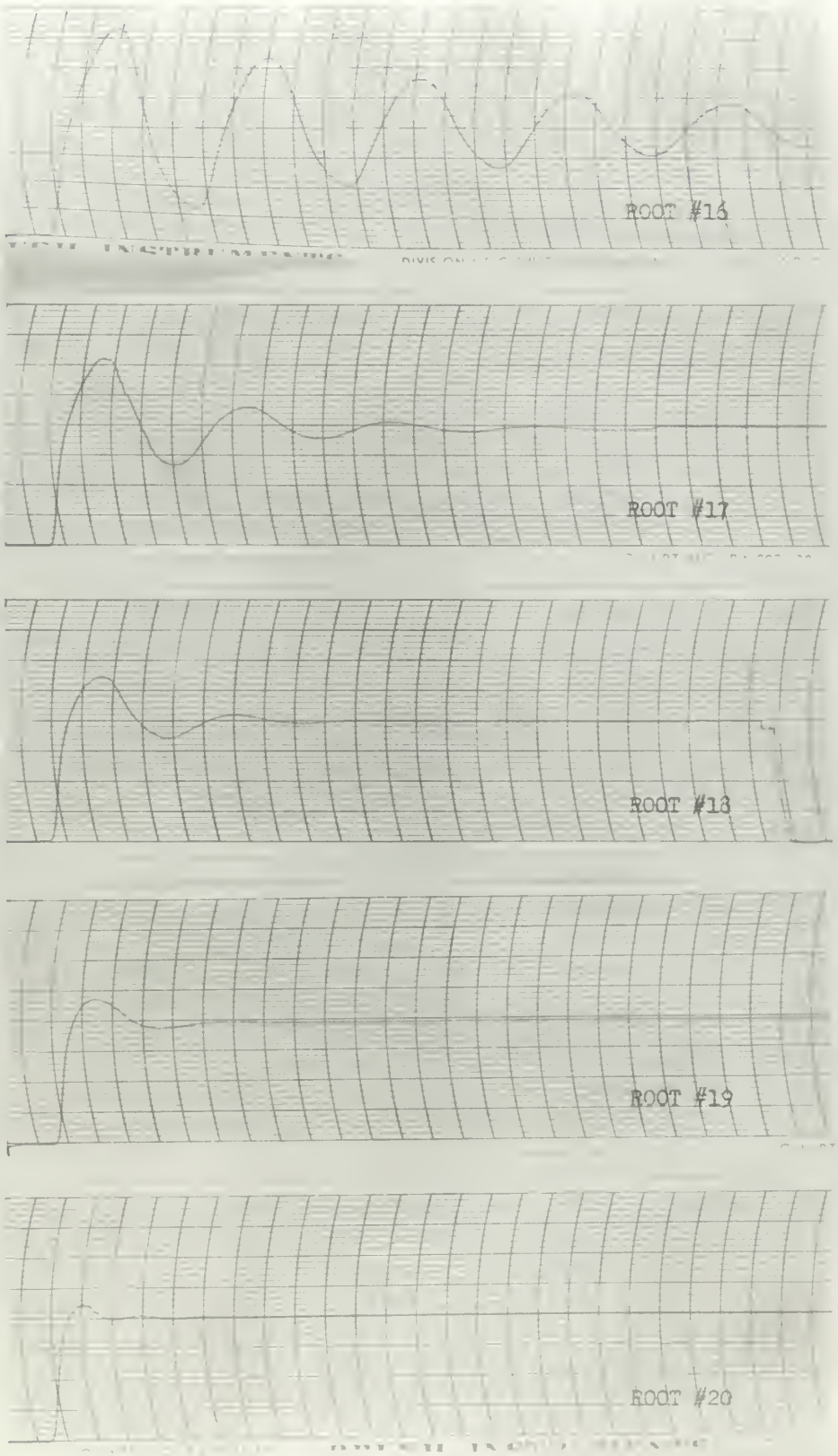


FIGURE 13. STEP RESPONSES ROOTS 16 - 20

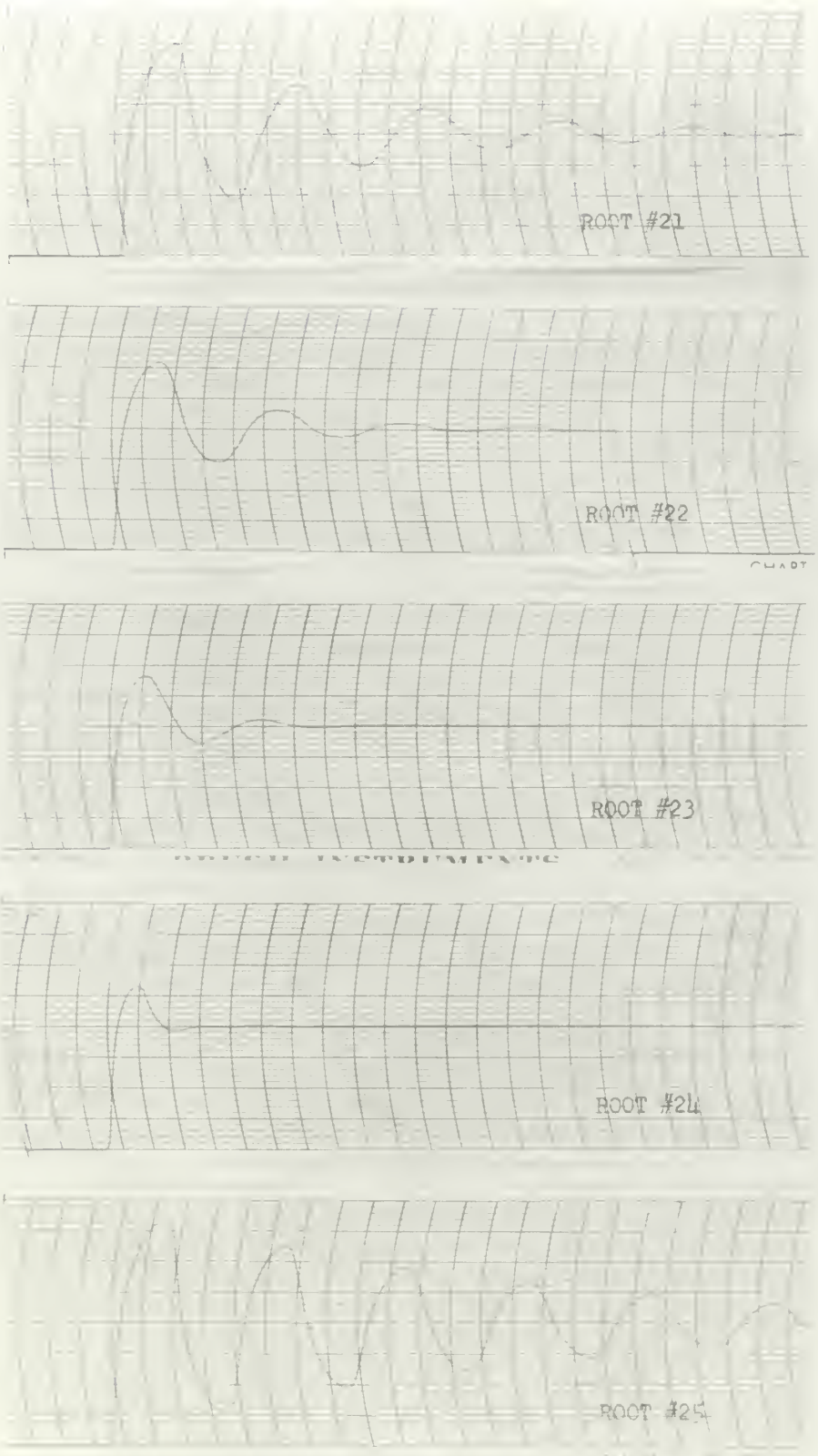


FIGURE 14. STEP RESPONSES ROOTS 21 - 25

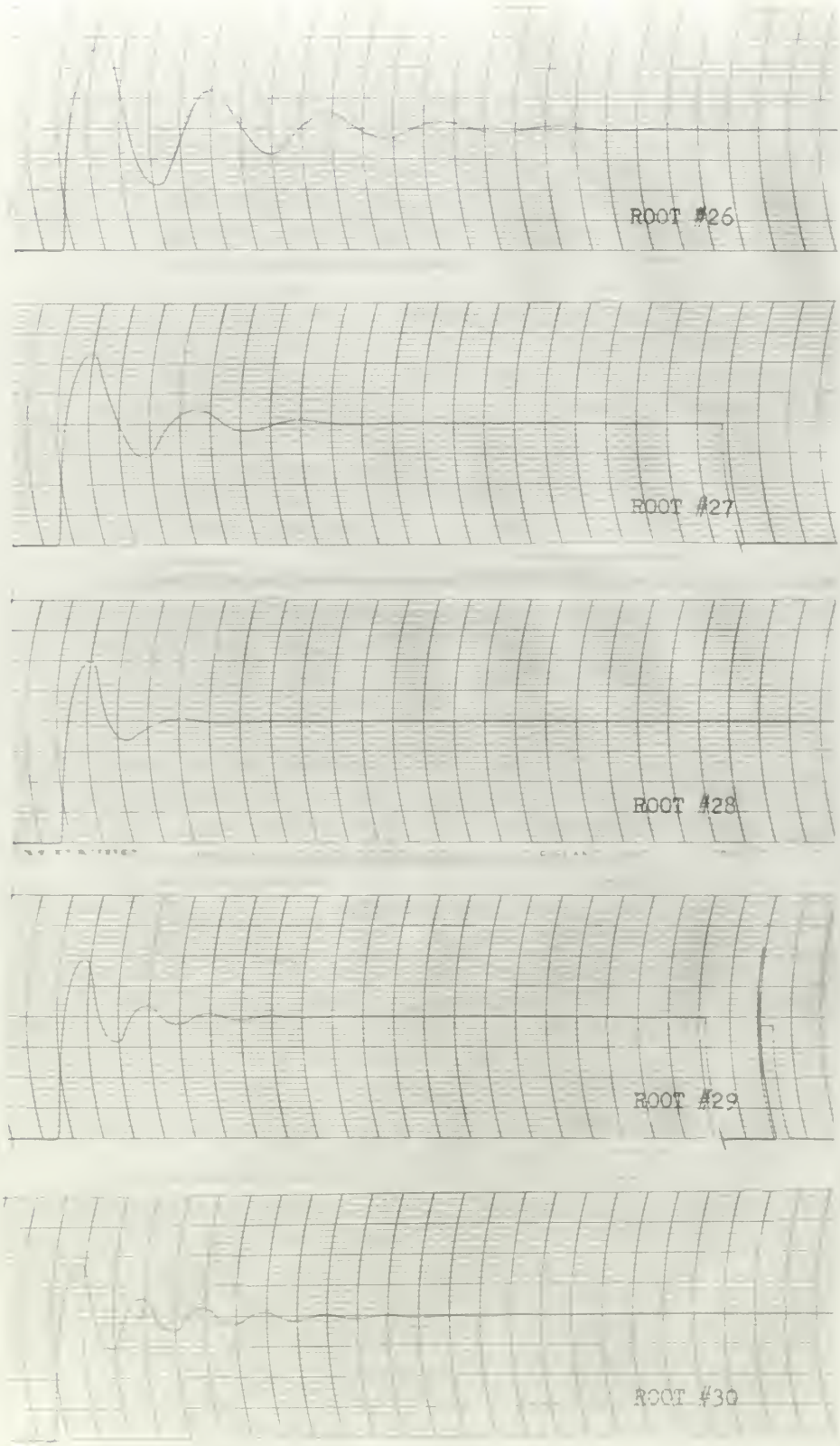


FIGURE 15. STEP RESPONSES ROOTS 26 - 30

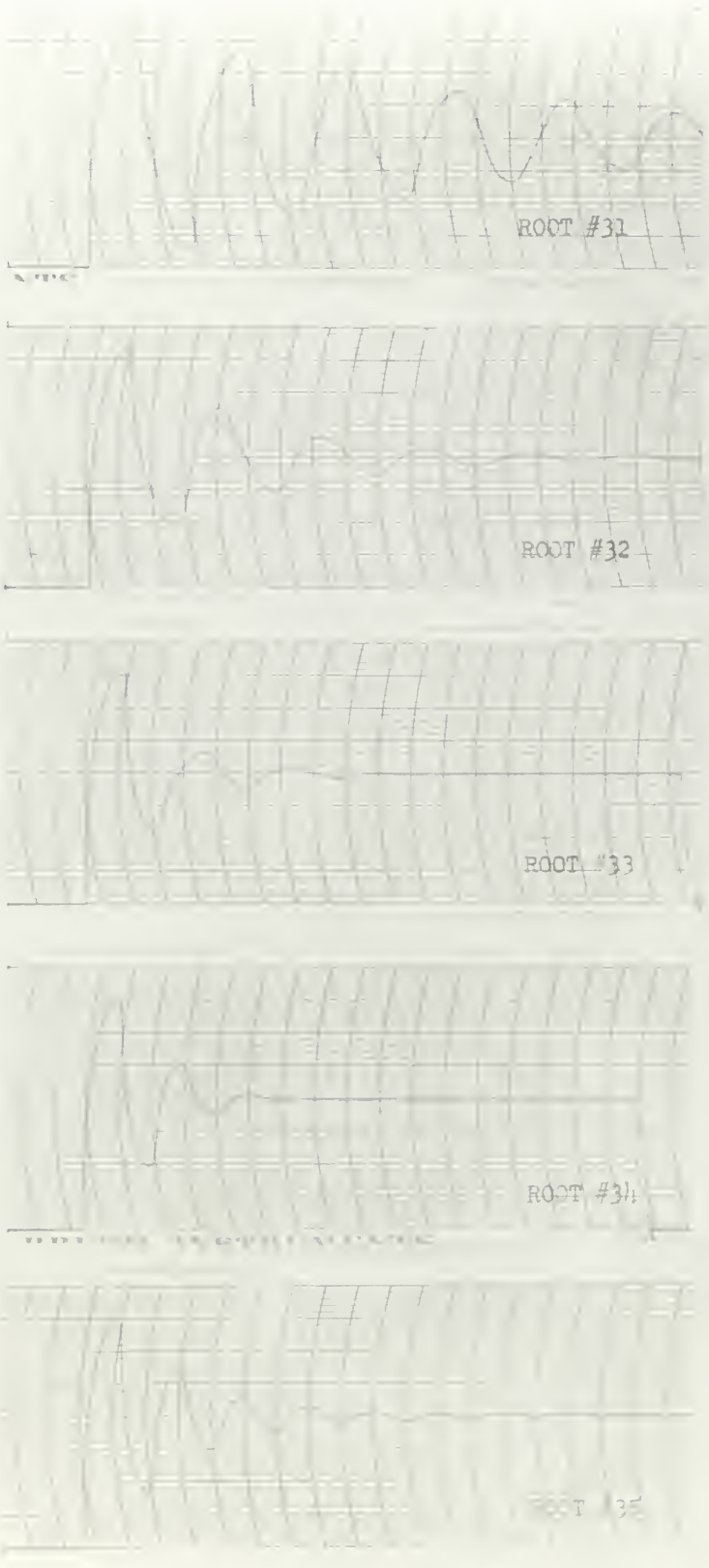


FIGURE 16. STEP RESPONSES ROOTS 31 - 35

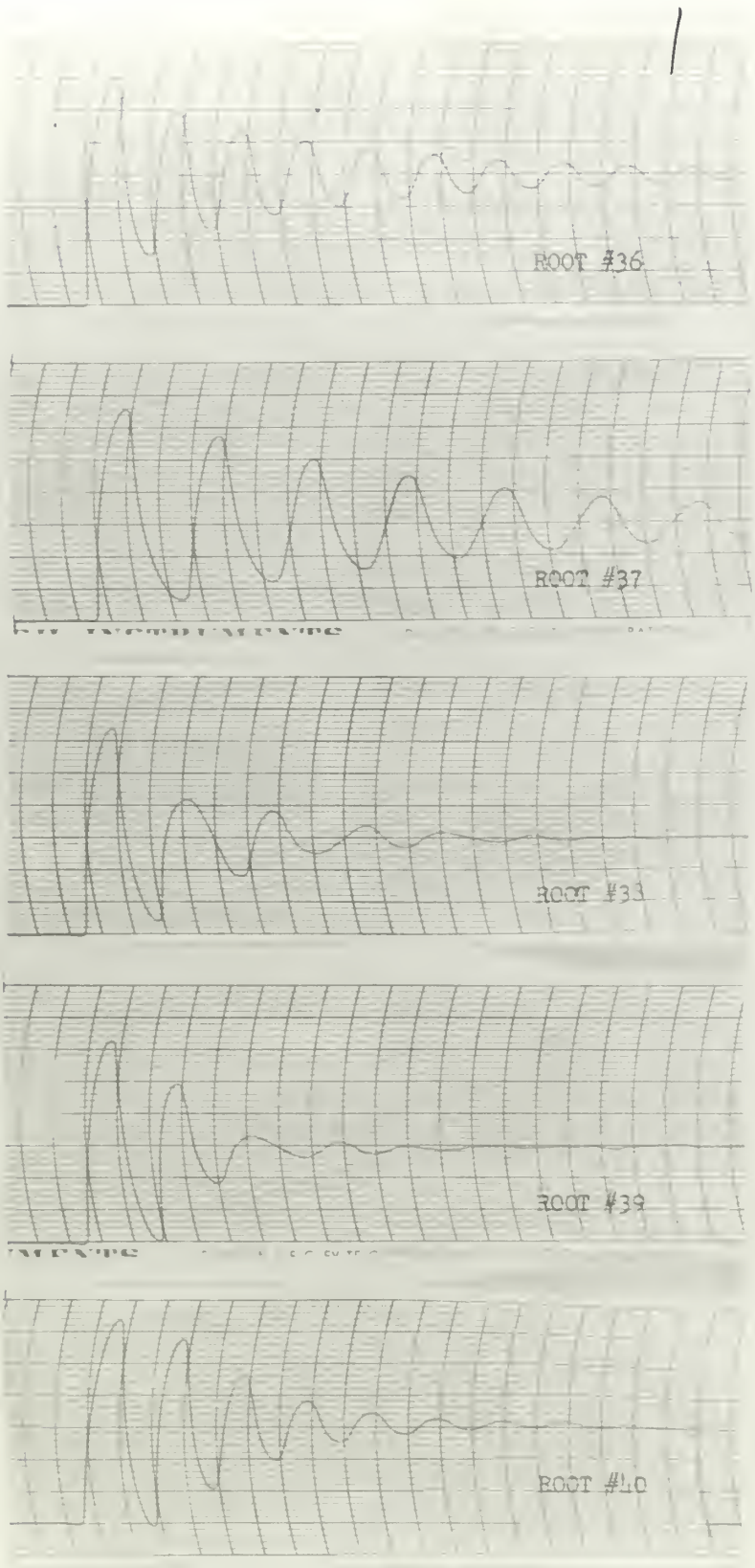


FIGURE 17. STEP RESPONSES ROOTS 36 - 40

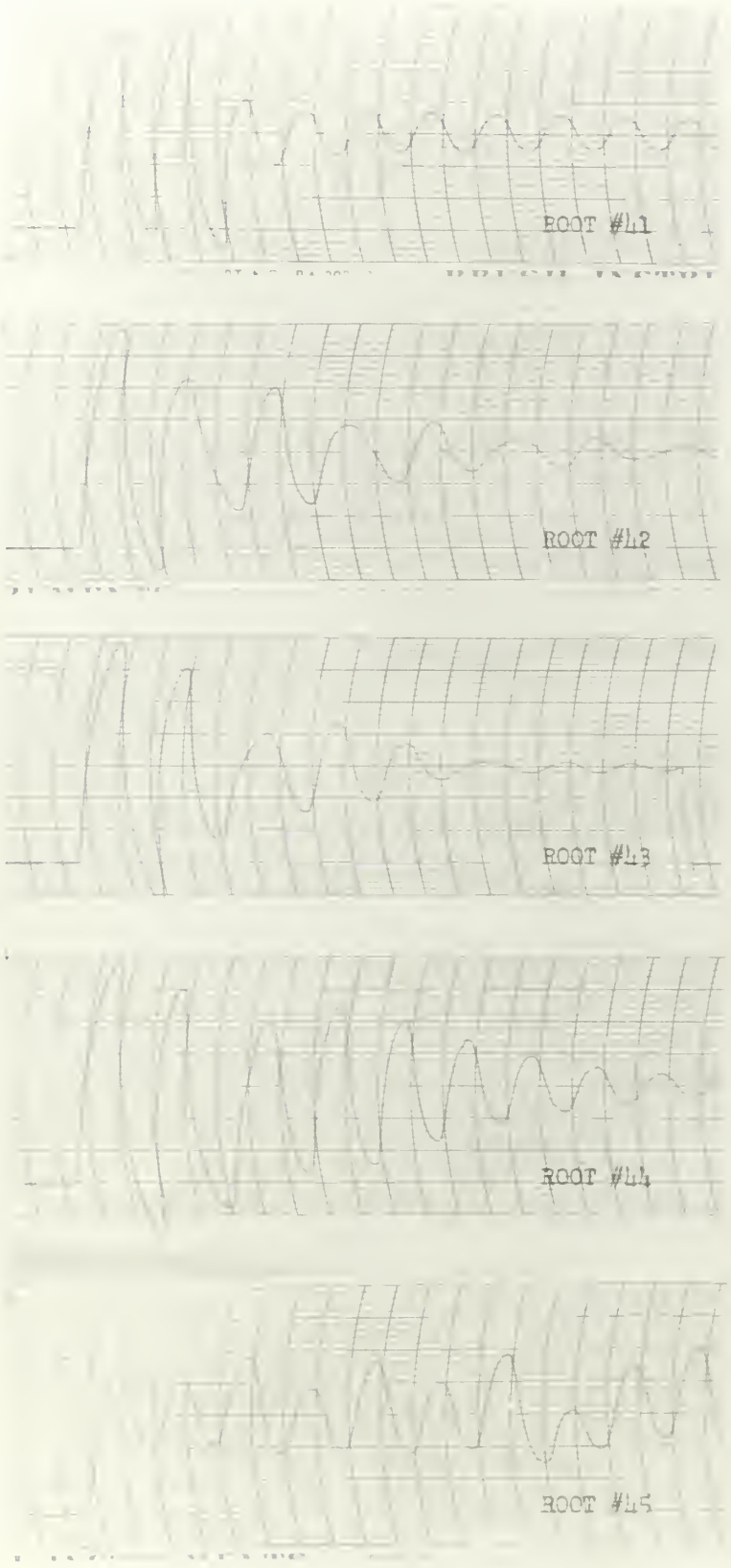


FIGURE 18. STEP RESPONSES ROOTS 41 - 45

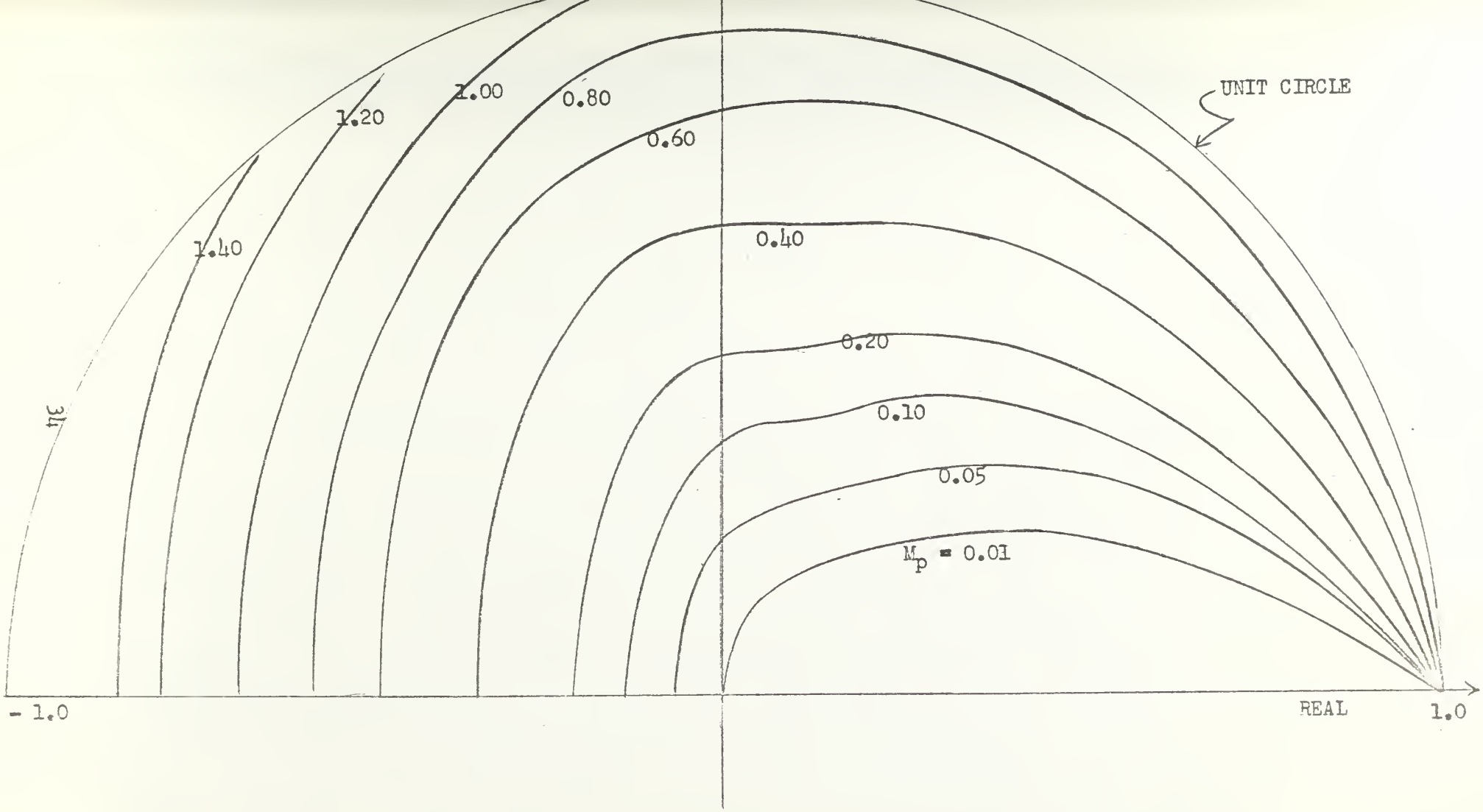
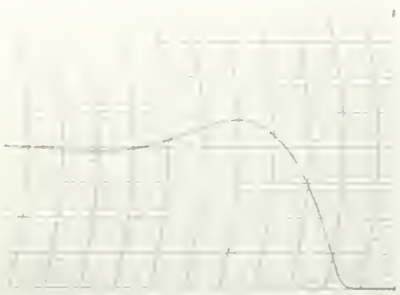
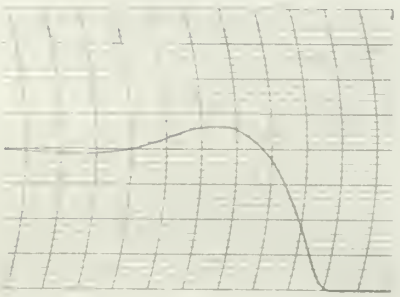


FIGURE 19. CONSTANT PEAK OVERSHOOT LOCT IN THE Z-PLANE

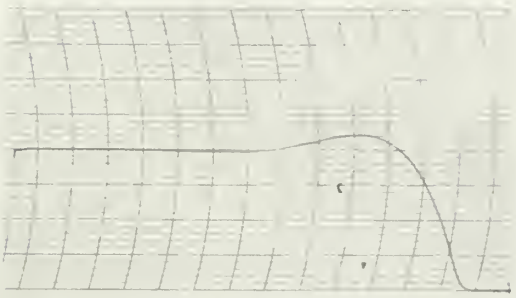


$\Delta\alpha$ = + 0.2 Re-compensated

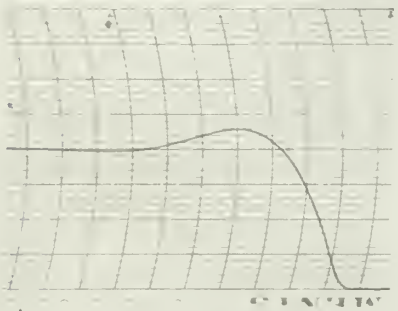
Original Compensation



$\Delta\alpha$ = + 0.1 Re-compensated

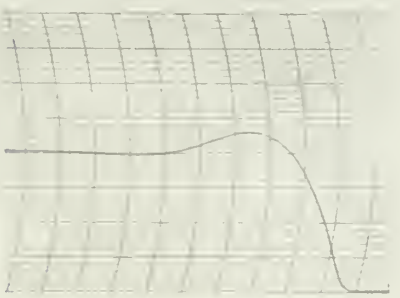


Original Compensation

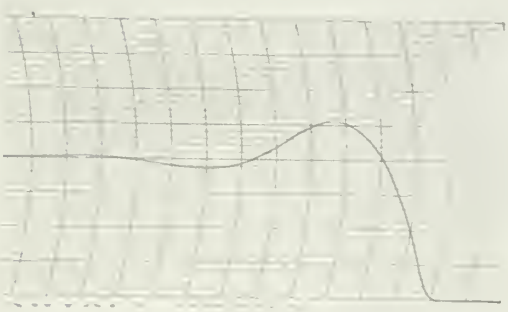


$\Delta\alpha$ = 0.0 No Re-compensation

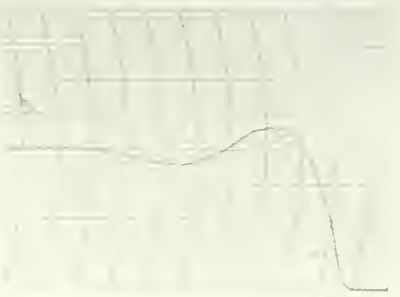
FIGURE 20. ZERO MIGRATION RESPONSES



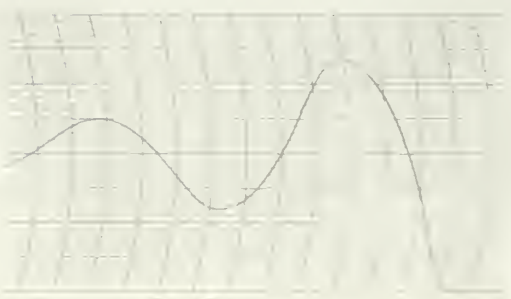
$\Delta\alpha$ = - 0.2 Re-compensated



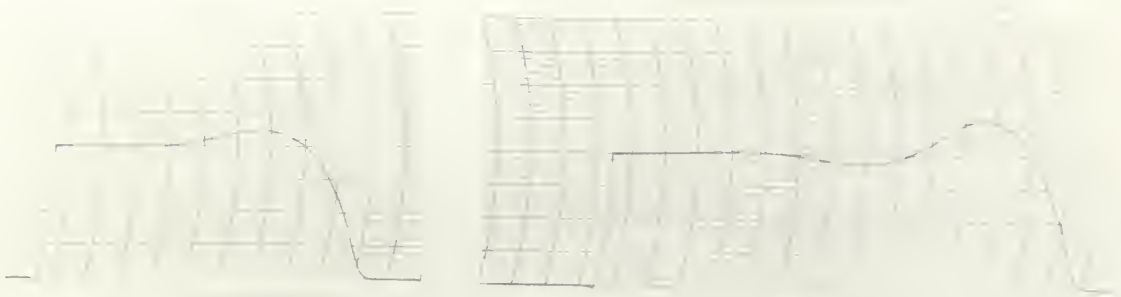
Original Compensation



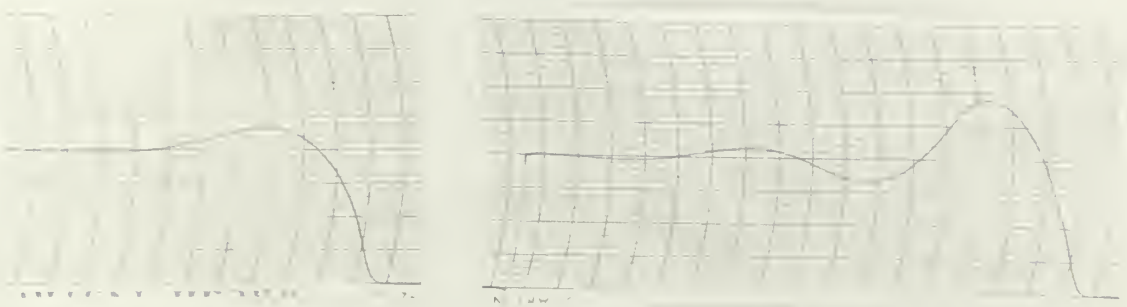
$\Delta\alpha$ = - 0.6 Re-compensated



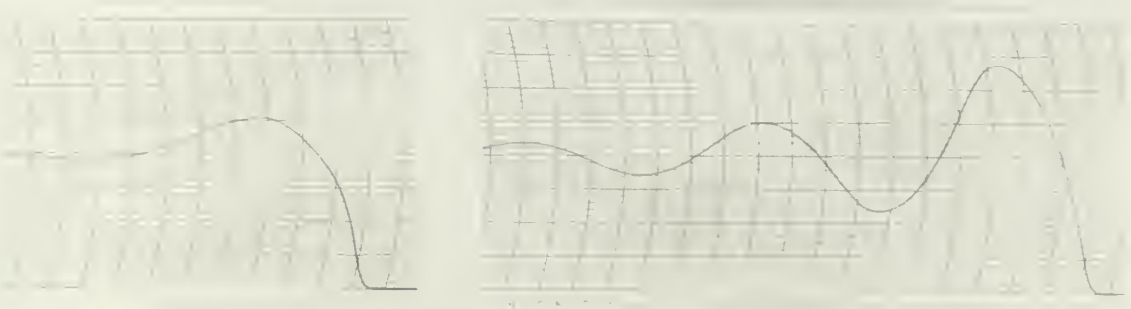
Original Compensation



$\Delta\alpha$ = - 0.2 Re-compensated Original Compensation



$\Delta\alpha$ = - 0.4 Re-compensated Original Compensation



$\Delta\alpha$ = - 0.6 Re-compensated Original compensation

FIGURE 21. POLE MIGRATION RESPONSES

CHAPTER 7

CONCLUSIONS

This investigation has concerned primarily with establishing the validity and usefulness of an analog simulation of a discrete compensator in a sampled-data system such as might be encountered when a digital computer is introduced into the servo loop. Other investigations of interest were the exploration of responses for various root locations in the z-plane, and a brief study of a simple adaptive system utilizing the discrete compensator. The conclusions may be summarized as follows:

(1) It is completely feasible to build an analog simulation of a discrete compensator of any order utilizing ordinary laboratory components, the order of the compensator being subject to the size of the computer available. The limits in accuracy are commensurate with those of the computer, and, in any case, are satisfactory for preliminary design work, averaging less than 5% in this investigation. If the digital computer being simulated has appreciable computation time, this can be simulated by using a diode bridge sampling switch triggered by a pulse delayed by the computation time.

(2) The simplicity of investigation of a wide variety of z-plane roots without the labor of modified z-transform calculations suggests an unlimited usefulness for the technique in practical and theoretical investigations into optimum compensation, intersampling ripple, self-adaption, etc.

(3) If the compensated system time constant changes due to external causes, and this change is known to be within certain limits and calculable from externally measured parameters, it might be possible to effect

by its zeroes. If the system being simulated were a servomotor, then as the motor's time constant changed, so would the apparent gain. This system could be re-compensated by the same formula mentioned above if the gain were programmed to remain constant as the time constant changed.

The investigation of the adaptive system was quite limited, and the possible usefulness of this method suggests that further investigation is warranted.

APPENDIX I

GRAPHICAL EXPLANATION OF DELAY CIRCUIT

The circuit of Fig. 6 can be considered to function in the following manner: Suppose there is a variable input signal such as shown in Fig. 22. Since at zero time there is no feedback signal, the error is the same as the input and the integrator starts integrating at the rate controlled by the error voltage (supplied by the sampler at $t = 0$), such that, assuming a linear integrator, at T seconds the integrator output is

$$T \times (\text{Error Voltage}) \times 1/T = \text{Error Voltage}$$

The feedback serves to progressively eliminate the error voltage. This can be seen at time $t = T$, where the sampled input voltage is the same as it was at $t = 0$, the feedback voltage is also the same magnitude but negative, and the error voltage goes to zero. The integrator holds its voltage with no error signal, and commences to integrate again at $t = 2T$, when it receives a new error signal. The integrator output sampled is thus seen to be the image of the input signal displaced one sampling period.

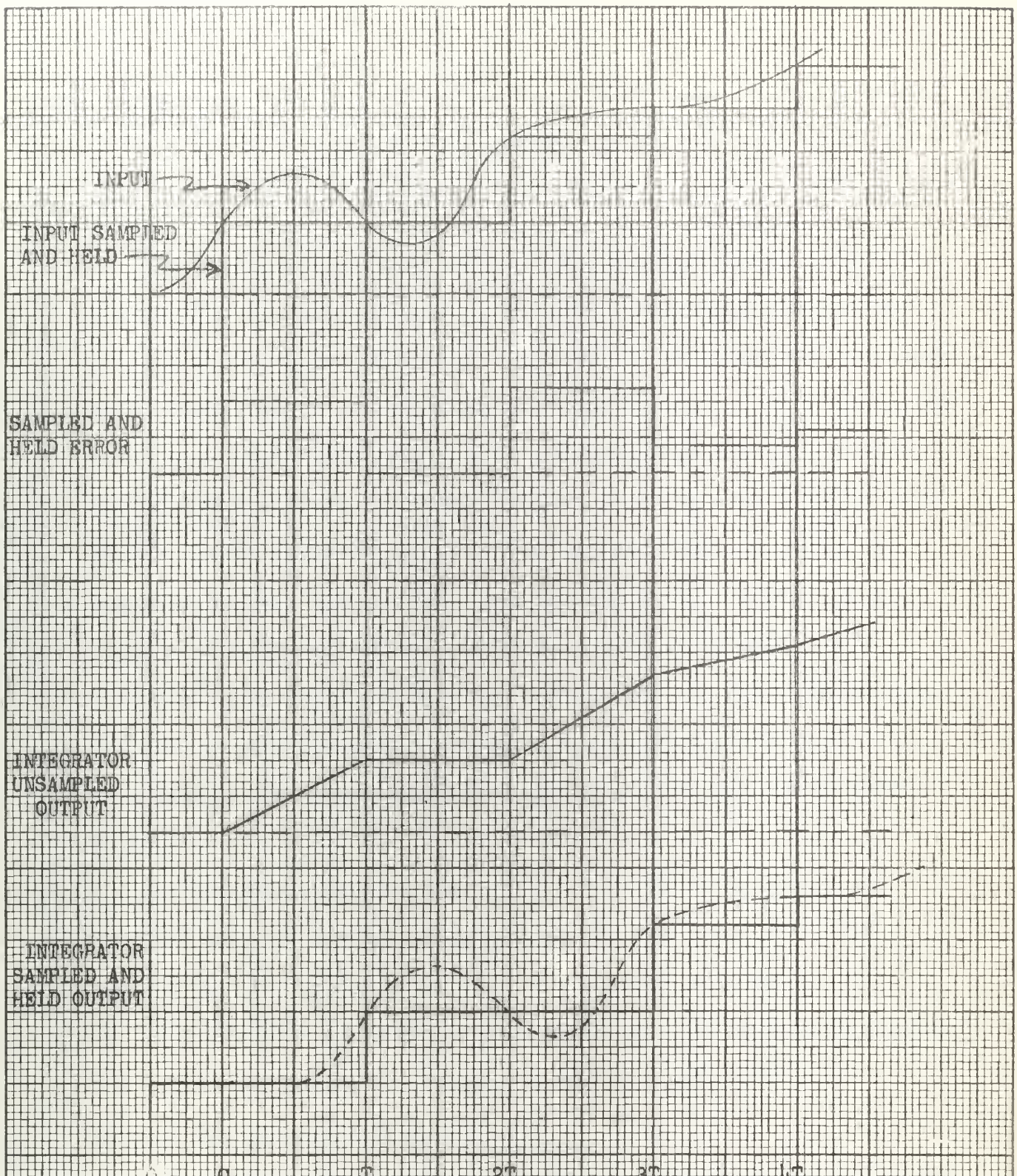

INPUT
INPUT SAMPLED AND HELD
SAMPLED AND HELD ERROR
INTEGRATOR UNSAMPLED OUTPUT
INTEGRATOR SAMPLED AND HELD OUTPUT
0
T
2T
3T
4T

FIGURE 22.

APPENDIX II

EQUIPMENT

Computer.

The Donner Scientific Co. Model 3000 electronic analog computer is a semi-portable, ten amplifier, unstabilized, relatively inexpensive computer which is generally used for elementary classroom and laboratory work. The computer has reasonably good characteristics for its size and cost. Each operational amplifier is a stable, high gain D.C. circuit, with a pentode driving a cathode follower. Average gain is better than 10,000. Input impedance is that of an open grid pentode, and output impedance is less than one ohm. Long term drift is - 4mv/hr. Output range is -100 to +100 volts, with load currents up to 5ma.

The Donner amplifiers were not satisfactory for use in the sampler and hold circuits, however, apparently due to excessive loading. For this purpose the chopper stabilized Philbrick Model USA - 3 was used.

Plotters.

All responses were recorded initially on the F. L. Moseley Co. AUTOGRAF Model 23 X-Y plotter running in the time sweep mode. This recorder permits measurements accurate to 1 part in 1,000.

The responses contained in this report were recorded on the Clevite Co. BRUSH dual channel recorder and amplifier Model RD5621.

Sampler and Zero-order Hold Circuit.

Figs. 23(a) and (b) contain the circuit diagrams of the sampler and zero-order hold circuit and the relay control circuit.

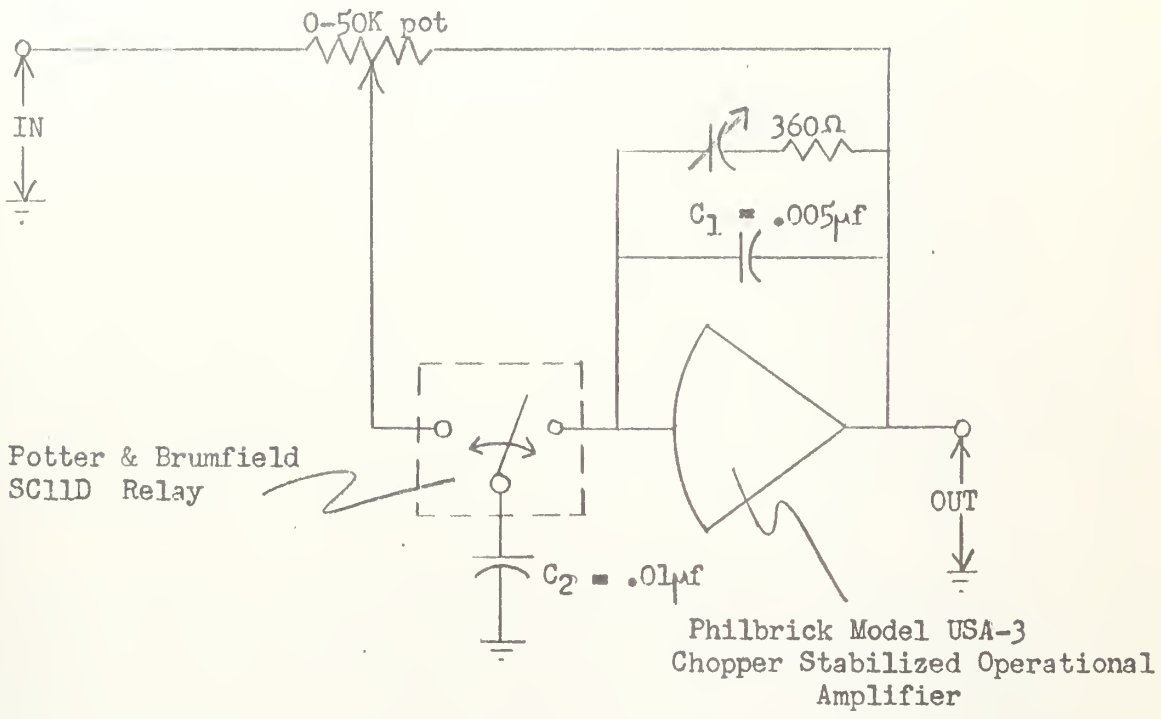


FIGURE 23 (a). SAMPLER AND HOLD CIRCUIT

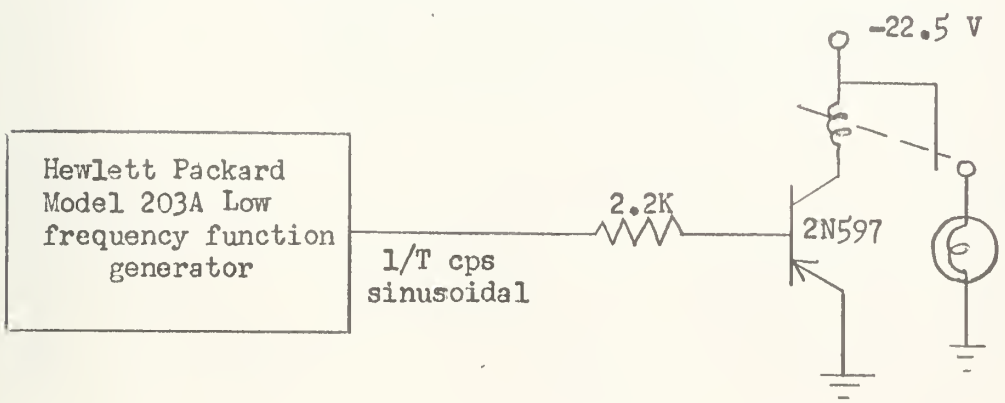


FIGURE 23(b). RELAY CONTROL CIRCUIT

The sampler and hold circuit is described in Appendix II. In order to account for the sign of a_1 and b_1, the sign changing amplifier #5 is either in or out of the circuit according to the following table:

a_1	b_1	Close broken circuit at (see Fig. 24)
+	+	(1)
+	-	(2)
-	+	(3)
-	-	(4)

TABLE II

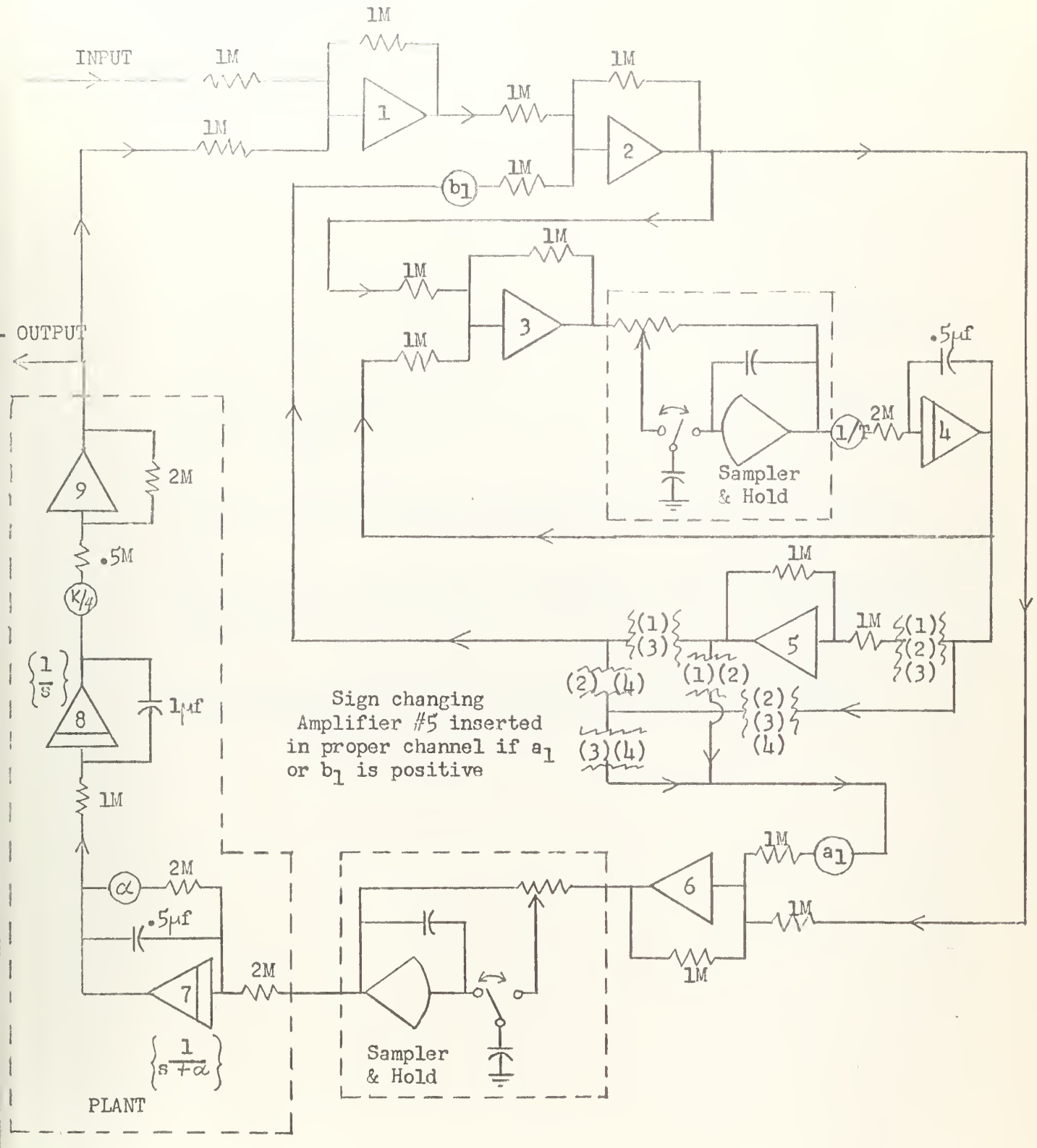


FIGURE 24. ANALOG COMPUTER CONFIGURATION USED IN INVESTIGATION

1. [illegible], J. R., and Franklin, G. F., Sampled-Data Control Systems, McGraw-Hill Book Co., New York, 1958.

2. Jury, E. I.; Sampled-Data Control Systems, John Wiley & Sons, New York, 1958.

3. Tou, J. T.; Digital and Sampled-Data Control Systems, McGraw-Hill Book Co., New York, 1959.

4. Barker, R. H.; The Pulse Transfer Function and Its Application to Sampling Servo Systems, Proceedings IEE, pt. IV, monograph 43, July 15, 1952.

5. Sklansky, J.; Network Compensation of Error-Sampled Feedback Control Systems, Columbia University Technical Report T-7/B, April 1, 1955.

6. Bigelow, S. C.; A Digital-Analog Controller for Sampled Data Systems, Columbia University Technical Report. T-36/B, July 22, 1959.

7. Bigelow, S. C.; Operating and Maintenance Instructions for Sampled Data Processing Unit, Columbia University Memorandum Report M-2/B, no date.

8. Dye, R. A.; Magnetic Variable Time Delay Line, Masters Thesis (unpublished), University of California, September, 1959.